

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEVIN B. LEIGH,
TUAN A. PHAM AND JASON W. WHITEMAN

Appeal 2007-0339
Application 09/872,600
Technology Center 2100

Decided: July 3, 2007

Before JOSEPH F. RUGGIERO, LANCE LEONARD BARRY, and
JEAN R. HOMERE *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

I. STATEMENT OF THE CASE

A Patent Examiner rejected claims 1-55. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

A. INVENTION

The invention at issue on appeal automatically switches control of a bus in a processor-based device. (Specification 1.) Although the motherboard of a server may include a small computer system interface ("SCSI") controller for controlling SCSI devices (e.g., hard drives) connected to the controller, an end-user may wish to incorporate alternate SCSI controller cards that provide different or additional features. (*Id.* 3-4.) Use of alternate SCSI controller cards also may enable the user to ensure uniformity among all his servers. (*Id.* 4.)

As aforementioned, the Appellants' invention automatically switches control of a bus in a processor-based device. In a server, more specifically, control of a bus is automatically switched from a controller mounted on a system board to a controller located on an optional expansion card upon connection of the expansion card to the board. Automatic switching includes isolating the on-board controller from the bus and appropriately terminating any transmission line ends on the bus resulting from the establishment of the alternative control path. (*Id.* 34.)

Claim 1, which further illustrates the invention, follows.

1. A method of switching control of a bus in a processor-based device, the method comprising the acts of:

electrically coupling a first bus controller to the bus;

generating a detection signal indicative of coupling of a second bus controller to the bus; and

automatically isolating the first bus controller from the bus in response to the detection signal.

B. REJECTIONS

Claims 1-10, 12-21, 23-31, 35-41, 44¹-50, and 52-55 stand rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,706,447 ("Vivo") and U.S. Patent No. 6,701,402 ("Alexandria"). Claims 11, 22, and 34 stand rejected under § 103(a) as obvious over Vivo; Alexandria; and the Appellants' admitted prior art ("AAPA"). Claims 32-34, 42, 43,² and 51 stand rejected under § 103(a) as obvious over Vivo; Alexandria; and U.S. Patent No. 6,701,402 ("Gasparik").

II. ISSUE

Rather than reiterate the positions of parties *in toto*, we focus on the issue therebetween. The Examiner admits that Vivo does not disclose "automatically isolating the first bus controller from the bus in response to the detection signal." (Answer 3.) He finds, moreover, "In Alexander, III et al. when the PCI bus controller gives control to one of the masters, the other masters are prevented from communicating with the disk controller and are thus 'isolated' from it." (*Id.* 18.) The Examiner further finds, "Alexander, III et al. further make specific mention in the abstract that the purpose of this

¹ Although the statement of this rejection includes claim 43, (Answer 3), the claim depends from claim 42, which stands rejected under Vivo, Alexandria, and U.S. Patent No. 6,701,402. (*Id.* 17.) Therefore, we treat claim 43 as rejected under the same latter combination of references.

² *Id.*

'isolation' is to avoid data collisions, data loss and possibly system failure as required by appellant's use of this term." (*Id.*)

The Appellants argue, "isolating the disk controller 110 from the other masters is *wholly different* from 'isolating the first bus controller *from the bus*' as recited in claim 1, for example. (Emphasis added). Contrary to what is recited in the claims, neither the disk controller 110, the controller 107, nor the other masters *are ever isolated from the bus*. Alexander, col. 3, lines 38-52." (Reply Br. 2.) Therefore, the issue is whether teachings from the prior art itself would appear to have suggested responding to a detection signal by automatically isolating a first bus controller from a bus.

In addressing the issue, the Board conducts a two-step analysis. First, we construe the independent claims at issue to determine their scope. Second, we determine whether the construed claims would have been obvious.

III. CLAIM CONSTRUCTION

Our analysis begins with construing the claim limitations at issue. "The Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582, 32 USPQ2d 1031, 1034 (Fed. Cir. 1994) (citing *In re Gulack*, 703 F.2d 1381, 1385, 217 USPQ 401, 403-04 (Fed. Cir. 1983)).

Here, claim 1 recites in pertinent part the following limitations:
"automatically isolating the first bus controller from the bus in response to the detection signal." Claims 13, 21, 23, 35, 44, 52, and 53 include similar limitations. Considering all these claim limitations, the independent claims require responding to a detection signal by automatically isolating a first bus controller *from a bus*.

IV. OBVIOUSNESS DETERMINATION

"Having determined what subject matter is being claimed, the next inquiry is whether the subject matter would have been obvious." *Ex Parte Massingill*, No. 2003-0506, 2004 WL 1646421, at *3 (B.P.A.I 2004). "In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) (citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)).
"A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, Alexander "illustrates a circuit 100, such as an integrated circuit [i.e., "IC"], in a host (e.g., server, work station, personal computer and the like) that allows a peripheral component interconnect (PCI) device 105 (e.g., a RAID or other conventional storage devices) to utilize a conventional disk controller 110 (e.g., an LSI 1030 SCSI controller) in the

host device." (Col. 2, ll. 46-52.) The IC "provides the peripheral device with sole access to the disk controller when operating in a straight mode. In [the] straight mode, the peripheral device may communicate with the disk controller through a PCI bus to perform operations, such as retrieving or writing data to the peripheral device." (Abs. ll. 5-10.) The abstract, to which the Examiner cites, *supra*, discusses isolating controllers from *the disk controller*. To wit, "in [the] straight mode, other controllers, including the host's CPU, may be prevented from using the disk controller to avoid data collisions, data loss and possible system failure." (*Id.* 10-13.)

We are unpersuaded, however, that the IC isolates the other controllers from the PCI bus. To the contrary, the reference explains that "because IDSEL 135 is disconnected from PCI bus 115, other devices . . . may become master of PCI bus 115 [although the other devices] cannot detect disk controller 110 when they perform a configuration cycle." (Col. 3, ll. 46-49.) We agree with the Appellants aforementioned argument that "isolating the disk controller 110 from the other masters is *wholly different* from 'isolating the first bus controller *from the bus*'. . . ." (Reply Br. 2.)

V. CONCLUSION

Absent a teaching or suggestion of responding to a detection signal by automatically isolating a first bus controller from a bus, we are unpersuaded of a prima facie case of obviousness. Therefore, we reverse the rejection of claims 1, 13, 21, 23, 35, 44, 52, and 53 and of claims 2-10, 12, 12-20, 24-31, 36-41, 45-50, 54, and 55, which depend therefrom.

The Examiner does not allege, let alone show, that the addition of AAPA or Gasparik cures the aforementioned deficiency of Vivo and Alexandria. Therefore, we also reverse the rejections of claims 11, 22, 32-34, 42, 43, and 51.

The "Appellants respectfully request that the Board overturn the rejection and allow independent claims 1, 21, 23, 35, 44, 52, and 53, and the claims that depend therefrom." (Appeal Br. 15.) They also "request that the Board withdraw the obviousness rejections of claims 11, 22, and 34," (*id.* 20), and "withdraw the obviousness rejections in relation to claims 32-34, 42, and 51." (*Id.* 21.) "Additionally, [the] Appellants respectfully request that the Board direct the Examiner to allow these claims." (*Id.*)

In an *ex parte* appeal, however, the Board "is basically a board of review C we review . . . rejections made by patent examiners." *Ex parte Gambogi*, 62 USPQ2d 1209, 1211 (B.P.A.I. 2001). We lack authority to direct an examiner to withdraw an Office action or to allow claims. It is patent examiners who have the authority to withdraw their rejections, M.P.E.P. §§ 707.07(e), 1004, 1005 (8th ed., 4th rev. Oct. 1005),³ and to allow claims. *Id.* at §§ 1005, 1302.13.

³ We cite to the version of the Manual of Patent Examining Procedure in effect at the time of the Appeal Brief.

Appeal 2007-0339
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REVERSED

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